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(71)Applicant: MATSUSHITA ELECTRIC IND CO

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(72)Inventor: SHINOHARA KATSUYA

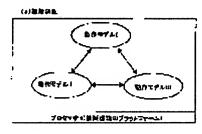
MIZUNO MASANOBU MOTOHARA AKIRA

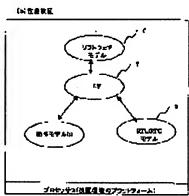
(54) SIMULATION DEVICE AND SIMULATION MODEL GENERATION PROGRAM

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a simulation device capable of performing performance verification retaining a possible abstraction degree of cache analysis on a single verification platform without requiring an ISS (instruction set simulator).

SOLUTION: A software-mounted function is generated as a software model 6 operated on a verification environmental platform (processor B), a hardwaremounted function is established as an RTL/RTC model 2 or an operation model higher in abstraction degree than it, and the performance verification is performed on the processor B. An interface model 7 for delivering input and output data between models is provided among the models.





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